IN THE SPECIFICATION

Please amend the paragraph beginning on page 22, line 12 as follows:

Figure 2 is a block diagram of an electronic system 200 that incorporates the present invention. The system 200 includes a conventional arrangement of a processor 202, with an instruction cache 204, a data cache 206, main memory arbitration 208, and main memory 210. The system speeds up dynamic array and dynamic overlay array access using a boundary policy enforcement and index mapping unit 220 and a Cached Dynamic Array (CDA) cache 222. Copending U.S. Application No. , 09/901811, Publication No. US-2003-0014588-A1 ~~(SLWK 303.743US1)~~ entitled CACHING OF DYNAMIC ARRAYS, assigned to Applicants' assignee and filed on July 10, 2001 ~~or near the same date as the present application~~, describes the dynamic array cache, and a cached dynamic array (CDA) system formed by the CDA cache and by the dynamic array and dynamic overlay code. The CDA cache 222 provides special hardware support that can be accessed through dynamic array code and an extended compiler to improve array accesses. As such, U.S. Application No. 09/901811, Publication No. US-2003-0014588-A1 ~~(SLWK 303.743US1)~~ is hereby incorporated by reference.